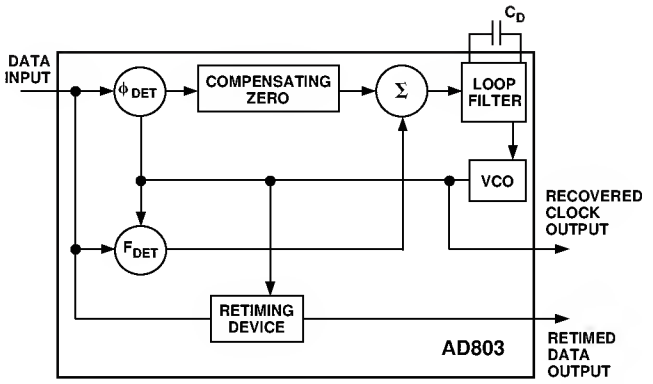
Clock Recovery and Data Retiming Phase-Locked Loop

AD803

FEATURES

- Standard Products: 20.48 Mbps
- Accepts NRZ Data, No Preamble Required
- Recovered Clock and Retimed Data Output
- Phase-Locked Loop Type Clock Recovery—No Crystal Required
- Random Jitter: 3.0° rms
- Pattern Jitter: Virtually Eliminated
- Operating Temperature Range: –40°C to +85°C
- Single Supply Operation: +5 V
- TTL Compatible Inputs and Outputs
- Low Power Consumption: 185 mW Typical, 275 mW Maximum

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD803 employs a second order phase-locked loop architecture to perform clock recovery and data retiming on Nonreturn to Zero (NRZ) data. This architecture is capable of supporting data rates between 18 Mbps and 30 Mbps. The product described here is optimized for operation on 20.48 Mbps, a data rate used in Passive Optical Networks (PONs).

Unlike other PLL-based clock recovery circuits, the AD803 does not require a preamble, an external VCXO, or an external crystal to lock onto input data. The circuit acquires frequency and phase lock using two control loops. The frequency acquisition loop initially acquires the clock frequency of the input data. The phase-lock loop then acquires the phase of the input data, and ensures that the phase of the output signals track changes in the phase of the input data. The loop damping of the circuit is dependent on the value of a user selected capacitor; this defines jitter peaking performance and impacts acquisition time.

The AD803 exhibits 0.08 dB jitter peaking, and acquires lock-on random or scrambled data in 3×10^5 bit periods when using a damping factor of 5.

The inclusion of a precisely trimmed VCO in the device eliminates the need for external components for setting center frequency, and the need for trimming of those components. The VCO provides a clock output within ±20% of its center frequency in the absence of input data.

The AD803 exhibits virtually no pattern jitter due to the performance of the patented phase detector. Loop jitter measures 3.0° rms. The nominal jitter bandwidth for the AD803 is set to 0.1% of the center frequency. The jitter bandwidth is mask programmable.

The device operates from a single +5 V supply, and consumes 185 mW. The product accepts TTL level input signals, and outputs TTL level signals that can drive a fan out of 10 ACT or HCT CMOS inputs. The AD803 is specified to operate from 40°C to +85°C and is available in a 20-pin SOIC.

REV. 0

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AD803–SPECIFICATIONS (V_{CC} = V_{MIN} to V_{MAX}, V_{EE} = GND, T_A = T_{MIN} to T_{MAX}, Loop Damping Factor = 5, unless otherwise noted)

Parameter	Condition	Min	Typ	Max	Units
NOMINAL DATA RATE			20.48		Mbps
CAPTURE RANGE/TRACKING RANGE[1]		19.10		20.50	Mbps
STATIC PHASE ERROR	2^{23}–1 PRN Sequence		15		Degrees
OUTPUT JITTER	ρ = 1		2.5		Degrees rms
	2^{23}–1 PRN Sequence		3.0	5.8	Degrees rms
JITTER TOLERANCE	f = 10 Hz	795	955		UI p-p
	f = 100 Hz	79.5	95.5		UI p-p
	f = 1 kHz	7.95	9.55		UI p-p
	f = 10 kHz	0.95	1.1		UI p-p
JITTER TRANSFER					
Damping Factor Capacitor, C_D	ζ = 1, Nominal		15		nF
Peaking			1.6		dB
Bandwidth			34		kHz
Damping Factor Capacitor, C_D	ζ = 5, Nominal		0.47		µF
Peaking			0.06		dB
Bandwidth			28		kHz
Damping Factor Capacitor, C_D	ζ = 10, Nominal		1.5		µF
Peaking			0.02		dB
Bandwidth			28		kHz
RECOVERED CLOCK SKEW	CLKOUT to DATAOUT Rising Edge		5.5	13.6	ns
	CLKOUT to DATAOUT Falling Edge	1.95			ns
TRANSITIONLESS DATA RUN	500-Bit Period Block		5.0		Degrees
Phase Drift	1000-Bit Period Block		10.0		Degrees
ACQUISITION TIME	ρ = 1/2		300,000		Bit Periods
POWER SUPPLY					
Voltage (V_{MIN} to V_{MAX})		4.5	5.0	5.5	Volts
Current	T_A = +25°C, V_{CC} = +5.0 V		40	50	mA
				60	mA
INPUT VOLTAGE LEVELS					
Input Logic High, V_{IH}	V_{CC} = +5 V ± 5%	2.0			Volts
Input Logic Low, V_{IL}				0.8	Volts
OUTPUT VOLTAGE LEVELS	V_{CC} = +5 V ± 5%				
Output Logic High, V_{OH}	I_{OH} = –0.4 mA	2.4			Volts
Output Logic Low, V_{OL}	I_{OL} = 4 mA			0.43	Volts
INPUT CURRENT LEVELS					
Input Logic High, I_{IH}			–0.06		mA
Input Logic Low, I_{IL}			–0.65		mA
OUTPUT SLEW TIMES, CLKOUT					
Rise Time, t_R	10%–90%		11	15.7	ns
Fall Time, t_F	90%–10%		5	6.9	ns
OUTPUT SLEW TIMES, DATAOUT					
Rise Time, t_R	10%–90%		13	18.2	ns
Fall Time, t_F	90%–10%		5.7	8.6	ns
SYMMETRY					
Recovered Clock Output			±5%		Deviation from 50%

NOTES

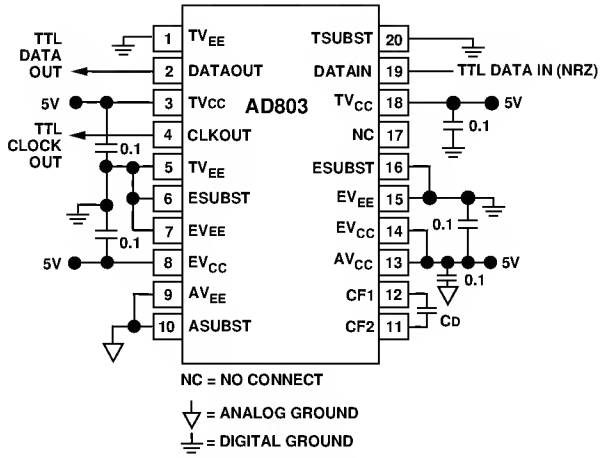
[1]No input jitter is applied to the input data for this specification.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltages ..... +7.5 V
Input Voltage (Pin 19 to V_{CC}) ..... +300 mV
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature Range (Soldering 60 see) ..... 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect device reliability.



Application/Test Circuit

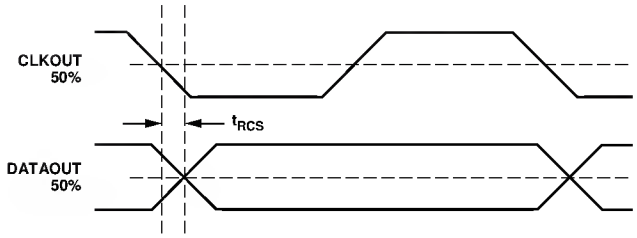
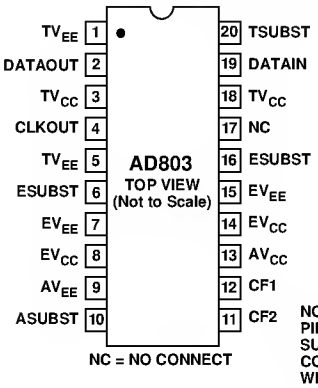


Figure 1. Recovered Clock Skew (See Specifications)

PIN CONFIGURATION



NOTES:
PINS 6 & 16 ARE DIGITAL SUBSTRATE AND SHOULD BE CONNECTED TO PINS 7 & 15, WHICH ARE DIGITAL V_{EE}.
PIN 10 IS ANALOG SUBSTRATE AND SHOULD BE CONNECTED TO PIN 9 WHICH IS ANALOG V_{EE}.

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	TV_{EE}	Digital Ground
2	DATAOUT	Retimed Data Output
3	TV_{CC}	Digital V_{CC}
4	CLKOUT	Recovered Clock Output
5	TV_{EE}	Digital Ground
6	ESUBST	Digital Substrate
7	EV_{EE}	Digital V_{EE}
8	EV_{CC}	Digital V_{CC}
9	AV_{EE}	Analog V_{EE}
10	ASUBST	Analog Substrate
11	CF2	Loop Damping Capacitor Input
12	CF1	Loop Damping Capacitor Input
13	AV_{CC}	Analog V_{CC}
14	EV_{CC}	Digital V_{CC}
15	EV_{EE}	Digital V_{EE}
16	ESUBST	Digital Substrate
17	NC	No Connection
18	TV_{CC}	Digital V_{CC}
19	DATAIN	Data Input
20	TSUBST	Digital Substrate

ORDERING GUIDE AND THERMAL CHARACTERISTICS

Model	Description	Operating Temperature	θ_{JA}	Package Option
AD803-20BR	20-Pin SOIC	–40°C to +85°C	75°C/W	R-20

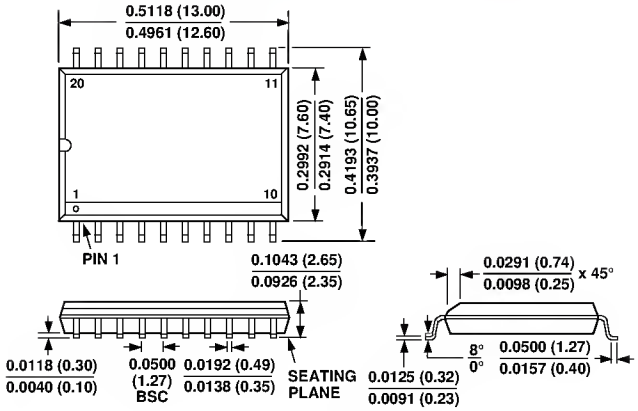
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD803 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-Pin Small Outline IC Package (R-20)



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